Patent
257/265

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Larry Leighton et al.

Serial No.: 09/813,604

Filed: March 20, 2001

Title: Bond Wire Tuning of Power Transistors and Amplifiers

Group Art Unit: 2826

Examiner: Johannes P. Mondt

AMENDMENT AFTER FINAL UNDER 37 CFR 1.116

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In response to the Office Action mailed July 3, 2002, please amend the application as follows:

In the Claims:

1. (Amended) A method of manufacturing a power transistor circuit, comprising carrying out the following steps in the enumerated order:

(1) securing a die to a substrate, the die comprising a transistor having an input terminal;

(2) measuring a performance characteristic of the transistor;

B1 Concl'd

(3) using one or more wires to electrically couple the transistor input terminal to an input matching element, an input signal lead, or both; and

(4) setting the impedance of the one or more wires based at least in part on the measured transistor performance characteristic from step (2).

Sub C2

5. (Amended) A method of manufacturing a power transistor circuit, comprising carrying out the following steps in the enumerated order:

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(1) securing a die to a substrate, the die comprising a transistor having an output terminal;

(2) measuring a performance characteristic of the transistor;

(3) using one or more wires to electrically couple the transistor output terminal to an output matching element, an output signal lead, or both; and

(4) setting the impedance of the one or more wires based at least in part on the measured transistor performance characteristic from step (2).

Sub C3

9. (Amended) A power transistor circuit, comprising:

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a substrate;

a die secured to the substrate, the die comprising a transistor having an input terminal;

one or both of an input lead and an input matching element secured to the substrate; and

B3 Concld

one or more wires electrically coupling the transistor input terminal to the one or both of the input matching element and input signal lead, wherein the impedance of the one or more wires is selected based at least in part on a performance characteristic of the transistor measured after the die is secured to the substrate.

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Sub C4

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13. (Amended) A power transistor circuit, comprising:

a substrate;

a die secured to the substrate, the die comprising a transistor having an output terminal;

10 one or both of an output lead and an output matching element secured to the substrate; and

one or more wires electrically coupling the transistor output terminal to the one or both of the output matching element and output signal lead, wherein the impedance of the one or more wires is selected based at least in part on a performance characteristic of the

15 transistor measured after the die is secured to the substrate.